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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,131	08/16/2001	Hyungwon Kim	UOM 0209 PUSP	3611

7590 04/28/2003

John S. Le Roy
Brooks & Kushman P.C.
22nd Floor
1000 Town Center
Southfield, MI 48075-1351

EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/931,131	KIM ET AL.
	Examiner	Art Unit
	Stacy A Whitmore	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ravi, "Approximation of decomposition of binary decision diagrams" in view of Pal, "Synthesis of two-level dynamic CMOS circuits".

2. As for claim 1, Ravi disclosed the invention substantially as claimed, including a method for synthesizing a circuit representation into a new circuit representation having greater unateness, the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit [pg. 3, section 3, first two paragraphs; pg. 4, section 3, figure 5];

(ii) recursively decomposing the representation of the at least one sub circuit [pg. 3, section 3, first two paragraphs; pg. 4, section 3, figure 5]; and

(iii) merging the representation into the circuit representation to form a new circuit representation [pg. 3, section 3, first two paragraphs; pg. 4, section 3, figure 5].

Ravi did not specifically disclose that the decomposition of the sub-circuit is decomposed into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit.

Pal disclosed decomposition of the sub-circuit is decomposed into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit [pg. 82, abstract; pg. 84 section 3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ravi and Pal because both Ravi and Pal disclose the decomposition of Boolean functions for the purpose of finding smaller representations of a circuit. Adding Pal's unate decomposition would aid Ravi's system by finding the minimum amount of gates in order to implement a circuit, which would improve clock skew of large circuits such as VLSI [see Pal, pg. 82, abstract; and pg. 86, section 4].

3. Claims 1-7, 10-16, 19-35, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brayton, R., "A multiple-level logic optimization system" in view of Pal, "Synthesis of two-level dynamic CMOS circuits".

4. As for claims 1, 10, 20, and 29, Brayton disclosed the invention substantially as claimed, including a method for synthesizing a circuit representation into a new circuit representation having greater unateness, the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit [pg. 1075, section B., lines 1-7];

(ii) recursively decomposing the representation of the at least one sub circuit into a sum-of-products or product-of-sums representation having a greater unateness than the representation of the at least one subcircuit [pg. 1067, section E.; pg. 1075-1076, section B. and pg. 1075, left hand side]; and

(iii) merging the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation [pg. 1067, section E.; pg. 1075-1076, section B. and pg. 1075, left-hand side].

[Claims 10, 20, and 29] means for receiving input defining the circuit representation, and outputting the new circuit representation [pg. 1063 and pg. 1079, section VII].

Brayton did not specifically disclose that the recursive decomposition has a greater unateness than the representation of the at least one subcircuit.

Pal disclosed decomposition with a greater unateness [pg. 84].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brayton and Pal because both Brayton and Pal disclose the decomposition of Boolean functions for the purpose of finding smaller representations of a circuit. Adding Pal's unate decomposition would aiding Brayton's system to find the smallest Boolean circuit representation without redundancies which would reduce overall circuit size.

5. As for claims 2, 11, 21, and 30, Pal further disclosed repeating steps (i), (ii) and (iii) until a desired level of unateness for the new circuit representation has been achieved.

6. As for claims 3, 7,12, 16, 22, 25, 31, and 35, Pal further disclosed wherein the sum-of-products or product-of-sums representation selected for each decomposition is the representation having fewer binate variables / [claim 7] the representation of the at least one sub-circuit is highly unate [pgs. 84, 86, AND 87; Pal disclosed the fewest binate variables because Pal's algorithm decomposes the function into functions that are unate and therefore not binate].

7. As for claims 4, 13, 23, and 32, Brayton further disclosed merging common expressions of the sum-of-products or product-of-sums representations [pg. 1076, resubstitution].

8. As for claims 5, 14, 24, and 33, Brayton further disclosed algebraic division is implemented to merge common expressions of the sum-of-products or product-of-sums representation [pg. 1075].

Brayton did not disclose that unate expressions are merged.

Pal disclosed the decomposition of unate expressions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brayton and Pal because merging Pal's unate expressions would improve Brayton's system by further reducing the circuit representations with the same functions, which would reduce overall circuit size.

9. As for claims 6 and 34, Brayton disclosed the circuit is a digital circuit [pg. 1063, section II.].

10. As for claims 19, 28, and 38, Brayton further disclosed wherein the circuit representation and the new circuit representation are input and output in a hardware description language [pg. 1063; and pg. 1079, section VII.].

11. Claims 8-9, 17-18, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brayton, R., "A multiple-level logic optimization system" in view of Pal, "Synthesis of two-level dynamic CMOS circuits", and further in view of Minato, "Fast factorization method for implicit cube set representation".

12. As for claims 8-9, 17-18, and 36-37, Brayton in view of Pal disclosed the invention substantially as claimed, including system for synthesizing a circuit representation having a greater unateness as cited above in claims 1, 10, 20, and 29.

Brayton in view of Pal did not disclose a (zero-suppressed) binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

Minato disclosed a (zero-suppressed) binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation [pg. 377, abstract, sections I. and II.A.; pg. 379, section III.; and pg. 383, section B].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brayton in view of Pal and Minato because merging Brayton in view of Pal's unate expressions would improve Brayton in view of Pal's system by allowing for the representation of very large cube sets in an efficient way in order to predict the behavior of such large circuits [See Minato, pg. 377, section I.].

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
April 24, 2003